PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	ZHENG et al.	Examiner:	Goudreau, G.
Serial No.:	Unknown	Group Art Unit:	1763
Filed:		Docket No.:	VLSI.225DIV1
Title:	OPTIMIZED METAL ETCH PROCESS TO ENABLE THE USE OF ALUMINUM PLUGS		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C 20231, on February 1, 2001.

By Lynda J. Bauer
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PRELIMINARY AMENDMENT FILED WITH A DIVISIONAL APPLICATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to commencing substantive examination of the above-identified application on the merits, please enter the following Preliminary Amendment.

In The Claims

Please cancel claims 1-26 and replace them with the following new claims:

27. *(New)* A semiconductor device comprising:

a first metal portion over a substrate;

a dielectric layer above the first metal portion;

a second metal portion above the dielectric layer;

a single-layer aluminum alloy plug extending from the first metal portion through the dielectric layer to the second metal portion, the plug having a first upper surface extending laterally beyond the second metal portion and substantially planar to an upper

surface of the dielectric layer and a second upper surface that extends above the first upper surface.

28. *(New)* The device of claim 27, wherein the single-layer plug does not exhibit an interface that would exist, were a first portion of the plug planarized before a remaining portion of the plug is formed.

29. *(New)* The device of claim 27, wherein the single-layer plug does not exhibit an interface that would exist, were a first portion of the plug subjected to chemical-mechanical polishing (CMP) before a remaining portion of the plug is formed.

30. *(New)* The device of claim 27, wherein the single-layer plug does not exhibit an interface that would exist, were a first portion of the plug etched before a remaining portion of the plug is formed.

31. *(New)* The device of claim 27, wherein the single-layer plug does not exhibit grain boundaries that would result from an internal interface between two portions of a plug formed during separate processes.

32. *(New)* The device of claim 27, wherein the single-layer plug exhibits properties that are about identical to those exhibited by a single-layer aluminum alloy plug formed using a continuous deposition process.

33. *(New)* The device of claim 27, wherein the dielectric layer is a single-layer dielectric.

34. *(New)* The device of claim 33, wherein the dielectric layer has an upper surface that does not exhibit surface characteristics that would exist, were the upper surface planarized using CMP.

35. *(New)* The device of claim 27, wherein the plug does not exhibit a void.

36. *(New)* The device of claim 27, wherein the second upper surface of the single-layer plug is substantially planar with a second upper surface of the dielectric layer.

37. *(New)* The device of claim 36, wherein the portion of the dielectric layer including the second upper surface has a side wall portion that is substantially aligned with a first side wall portion of the second metal layer, and wherein the portion of the plug including the second upper surface has a side wall portion that is substantially aligned with a second side wall portion of the second metal layer.

38. *(New)* A method of manufacturing a semiconductor device, the method comprising:

forming a plug comprising aluminum in a via extending from a first metal layer and through a dielectric layer in the device;

forming a second metal layer over the plug;

etching the second metal layer; and

over etching the second metal layer using an etch chemistry that etches the plug and the dielectric at an approximately equal rate.

39. The method of claim 38, wherein forming the second metal layer includes forming the second metal layer above the dielectric layer.

40. The method of claim 38, further comprising masking a portion of the second metal layer before etching the second metal layer, and wherein etching the second metal layer includes etching the unmasked portion of the second metal layer.

41. The method of claim 38, wherein etching the second metal layer with the first etch chemistry includes stopping etching when the plug is exposed.

42. The method of claim 41, wherein etching the second metal layer with the first etch chemistry includes stopping the etching just prior to the plug being exposed, and wherein overetching the second metal layer includes etching a remaining portion of the second metal layer at least until the plug is exposed.

43. The method of claim 42, wherein overetching the second metal layer includes etching at least a portion of the plug and the dielectric.

44. The method of claim 43, wherein the etched portions of the plug and the dielectric form an exposed surface that is about planar.

45. The method of claim 44, wherein a of the plug extends beyond the exposed surface.

46. The method of claim 38, wherein etching the second metal layer includes exposing the dielectric layer.

Remarks

A favorable reply is earnestly requested.

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